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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,683	09/25/2003	Yair Rosenbaum	SC0977EI	7557

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EXAMINER	
NGUYEN, HOAI AN D	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,683	ROSENBAUM ET AL.	
	Examiner	Art Unit	
	Hoai-An D. Nguyen	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7 and 10* is/are rejected.

7)☒ Claim(s) *3,4,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/25/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred form of claims of a utility application. These guidelines are suggested for the applicant's use.

Form of Claims

The claim or claims must commence on a separate physical sheet or electronic page and should appear after the detailed description of the invention. Any sheet including a claim or portion of a claim may not contain any other parts of the application or other material. While there is no set statutory form for claims, the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). If, at the time of allowance, the quoted terminology is not present, it is inserted by the Office of Patent Publication. Each claim begins with a capital letter and ends with a period. Periods may not be used elsewhere in the claims except for abbreviations. See Fressola v. Manbeck, 36 USPQ2d 1211 (D.D.C. 1995). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation, 37 CFR 1.75(i).

There may be plural indentations to further segregate subcombinations or related steps. In general, the printed patent copies will follow the format used but printing difficulties or expense may prevent the duplication of unduly complex claim formats.

Applicants are advised to see MPEP § 608.01(m) for more details.

Claim Objections

1. Claims 1, 3, 8 and 10 objected to because of the following informalities: where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. Appropriate correction is required.

Applicants are advised to see 37 CFR 1.75 and MPEP 608.01(i)-(p) for more details.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. (US 5,663,991 A) in view of Boateng (US 6,642,701 B2).

Kelkar et al. teaches an integrated circuit chip having built-in self measurement for PLL jitter and phase error comprising:

With regard to claims 1, 2 and 10, a test module (FIG. 1, system 10) for testing a phase locked loop circuit (Column 1, lines 8-11), the module comprising: phase detection means (FIG. 5, phase detector 88) for performing phase measurements of the phase locked loop circuit (From column 5, line 61 to column 6, line 6), frequency measurement means (FIG. 1, counters and a state machine 16) for performing frequency measurements of the phase locked loop circuit (From column 4, line 54 to column 5, line 2 and column 6, lines 52-64), and means (FIG. 2, edge

sorting circuit 20 and FIG. 5, calibration circuit 80) for performing calibration and jitter measurements (Column 3, lines 32-54 and from column 5, line 46 to column 6, line 35).

With regard to claim 2, the test module (FIG. 1, system 10) for testing a phase locked loop circuit and the phase locked loop circuit integrated in a single device (Column 2, lines 37-58).

Kelkar et al. teaches all that is claimed as discussed above, but they do not specifically teach the following:

- Analogue test means for testing at least one analogue element of the phase locked loop circuit.

However, Boateng teaches a device and method for testing phase-locked loops comprising:

With regard to claims 1, 2 and 10, the analogue test means (FIG. 1, connection control circuit 44) for testing at least one analogue element of the phase locked loop circuit (From column 3, line 58 to column 4, line 29).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the integrated circuit chip having built-in self measurement for PLL jitter and phase error of Kelkar et al. to incorporate the teaching of analogue test means for testing at least one analogue element of the phase locked loop circuit taught by Boateng since Boateng teaches that such an arrangement is beneficial to provide for a divide-and-conquer approach to develop a systematic method for testing PLLs that allows the digital circuit to be tested separately from the analog circuit as disclosed in column 4, lines 22-58.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. in view of Boateng as applied to claim 1 above, and further in view of Delmas (US 6,731,681 B1).

Kelkar et al. teaches an integrated circuit chip having built-in self measurement for PLL jitter and phase error having means (FIG. 2, edge sorting circuit 20 and FIG. 5, calibration circuit 80) for performing calibration and jitter measurements (Column 3, lines 32-54 and from column 5, line 46 to column 6, line 35), but they do not specifically teach the followings:

- The means for performing calibration and jitter measurements including a multiplexer arranged to receive the reference clock signal and a doubled reference clock signal from the phase locked loop circuit.

However, Delmas teaches a method for determining the frequency instability noise from a source, commonly called "jitter", and a device for implementing the method comprising:

With regard to claim 5, a multiplexer (multiplexer 2) arranged to receive the reference clock signal (reference signal CLKT) and a doubled reference clock signal (signal SB coming from the phase alignment loop 3 which has a signal CLKS as its input signal) from the phase locked loop circuit (Column 2, lines 25-34).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the integrated circuit chip having built-in self measurement for PLL jitter and phase error of Kelkar et al. and Boateng to incorporate the teaching of the means for performing calibration and jitter measurements including a multiplexer arranged to receive the reference clock signal and a doubled reference clock signal from the phase locked loop circuit taught by Delmas since Delmas teaches that such an arrangement is

beneficial to provide for a device, for measuring the frequency instability noise, that eliminates the necessity to directly measure the noise at the source output so that it can provide a highly accurate measurements as disclosed in column 2, lines 9-10 and column 3, lines 7-30.

Kelkar et al. teaches all that is claimed as discussed above, including the followings:

With regard to claim 6, the means for performing calibration and jitter measurements (FIG. 2, edge sorting circuit 20) includes a series of delay blocks (FIG. 2, delay elements 33, 35, 37 and 39) arranged as a ring circuit, each of the delay blocks providing a delayed output to a decoder (FIG. 1, decoder circuit 14) (FIG. 2 in view of FIG. 1 and column 3, lines 19-31 and from column 3, line 62 to column 4, line 24).

With regard to claim 7, each of the delay blocks is formed by inverters (FIG. 5 in view of FIG. 2 and column 5, lines 46-61). Kelkar et al. do not specifically teach that each of the delay blocks is formed by four inverters, but it would have been obvious to one having ordinary skill in the art at the time the invention was made to select a correct number of inverters to form a delay block to ensure that the total delay is the sum of the inverter delays as disclosed in column 5, lines 46-61.

Allowable Subject Matter

5. Claims 3, 4, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, claims 3 and 8 would be allowable if rewritten or amended to overcome the objections, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter:

- The primary reason for the indication of the allowability of claim 3 is the inclusion therein, in combination as currently claimed, of the limitation of the phase detection means comprising a reference clock path having first delay means and first latch means coupled to receive a reference clock signal from the phase locked loop circuit, and a feedback clock path having second delay means and second latch means coupled to receive a feedback clock signal from the phase locked loop circuit, wherein the first latch means is latched by the feedback clock signal and the second latch means is latched by the reference clock signal. This limitation is found in claim 3 is neither disclosed nor taught by the prior art of record, alone or in combination.
- The primary reason for the indication of the allowability of claim 8 is the inclusion therein, in combination as currently claimed, of the limitation of the analogue test means comprising a test controller arranged to perform testing of the at least one analogue element; a first digital-to-analogue converter coupled to the test controller and arranged for providing a first analogue output; and a second digital-to-analogue converter coupled to the test controller and arranged for providing a second analogue output, wherein the first and second analogue outputs are used in combination to test the at least one analogue element. This limitation is found in claim 8 is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's attention is invited to the followings whose inventions disclose similar devices.

- Wong et al. (US 5,295,079 A) teach digital testing techniques for very high frequency phase-locked loops.
- Watanabe et al. (US 6,522,122 B2) teach a jitter measuring device and method.
- Variyam et al. (US 6,661,266 B1) teach an all digital built-in self-test circuit for phase-locked loops.
- Suzuki (US 6,812,759 B2) teaches a DLL circuit capable of preventing locking in an antiphase state.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai-An D. Nguyen whose telephone number is 571-272-2170. The examiner can normally be reached on M-F (8:00 - 5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

ANJAN DEB
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoai-An D. Nguyen
Examiner
Art Unit 2858
HADN

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